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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/440,795	11/15/1999	CHRISTOPHER ALAN ADKINS	LE9-99-140	3446

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EXAMINER	
MILLER, PATRICK L	

ART UNIT	PAPER NUMBER
2837	

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/440,795	ADKINS ET AL.	
	Examiner	Art Unit	
	Patrick Miller	2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17,19-24 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,8,10,17,19-21,23,24,26 and 32* is/are rejected.

7)☒ Claim(s) *2,5-7,9,11-16,22 and 27-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 11 and 12 of the amendment filed on 11/24/03, with respect to the rejection(s)of claim(s) 1 under 35 USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Carobolante (5,572,099) and Seto (4,639,649).

Claim Objections

2. Claims 1, 11, 29, 30, 31, and 32 are objected to because of the following informalities: See bullets below. Appropriate correction is required.

   - Claims 1, 11, 31, and 32 cite a second occurrence of "a DC motor" (third line of claims). Change "a" to "the."
   - Claim 11 misspells "carriage" as "carnage." Please correct (sixth line of claim).
   - Claims 29 and 30 cite a second occurrence of "an inkjet print head" (third line of claims). Change "an" to "the."

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3, 4, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carobolante (5,572,099) in view of Seto (4,639,649).

- Carobolante discloses a control system for a DC motor comprising: a movement detector that outputs a feedback signal (col. 1, lines 39-43; FB is indicates motor speed, which is indicative of motor movement), a digital phase detector that compares the feedback signal with a reference phase signal (fig. 2, #2), and a digital loop filter that filters the compared signal (fig. 2, #5).
- Carobolante does not disclose that the digital phase detector follows a describing function to model non-linear components of the reference signal.
- Seto discloses a phase detector that follows a describing function to model non-linear components of the reference signal. The motivation to do so it to produce a beat signal which is compared to a specific frequency. This provides the advantage of improving synchronous operation of the motor (col. 1, lines 46-61).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the digital phase detector of Carobolante so it follows a describing function to model non-linear components of the reference signal, thereby

providing the advantage of improving synchronous operation of the motor, as taught by Seto.

- With respect to claim 3, a person with ordinary skill in the art would know a digital phase detector and a digital loop filter could be implemented in an application specific integrated circuit (ASIC).
- With respect to claim 4, the frequency detector is a phase-frequency detector (col. 1, lines 46-49).

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carobolante and Seto as applied to claims 1 and 4 above, and further in view of Trachtenberg (6,121,747).
   - Carobolante and Seto do not disclose the phase frequency detector having a memory.
   - Trachtenberg discloses a phase frequency detector including an edge-controlled digital memory network, having a plurality of states. Further, the network makes transitions among the plurality of states responsive to the reference and feedback signals input to the comparator, and the signal generated by the comparator is dependent on the state of the network, and the automatic phasing device controls the transitions among the states (col. 7, lines 6-17). This provides the advantage of driving a low-frequency pulse modulated signal that is supplied to the motor.
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the phase frequency detector of Carobolante and Seto with memory based on the reference signal, thereby providing the advantage of outputting a low-frequency signal to drive the motor, as taught by Trachtenberg.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carobolante and Seto as applied to claim 1 above, and further in view of Lundberg et al (5,811,998).

   - Carobolante discloses the digital phase detector being a phase-frequency detector (col. 1, lines 46-49), but Carobolante and Seto do not disclose the digital filter being a compensator that is set by a digital clock.
   - Lundberg et al disclose a digital filter that is an up/down counter configured to function as a digital integrator (digital compensator) (fig. 6, #138 including #140), whereby the digital integrator is controlled by a clock (fig. 6, #139). The motivation to provide a digital integrator as described is to integrate the occurrences of the phase condition. This provides the advantage of enabling phase expansion (col. 7, lines 14-25).
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention that the digital filter of Carobolante and Seto could be a digital integrator (compensator), thereby providing the advantage of enabling phase expansion, as taught by Lundberg et al.

6. Claims 17, 19, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (4,637,307) in view of Seto (4,639,649) and Carobolante (5,572,099).

   - Miller discloses a control system and method for controlling a print head comprising: a velocity detector that outputs a feedback signal (fig. 1, #40), a phase frequency detector that compares the feedback signal with a reference signal and outputs a comparison signal (fig. 2, #100), and a motor that controls the velocity of the printer head (fig. 2, #22).

- Miller does not disclose the frequency detector following a describing function and a filter that filters the comparison signal.
- Seto discloses a phase detector that follows a describing function to model non-linear components of the reference signal. The motivation to do so it to produce a beat signal which is compared to a specific frequency. This provides the advantage of improving synchronous operation of the motor (col. 1, lines 46-61).
- Carobolante discloses a filter that "filters" the output of a phase detector (fig. 2, #5). A person of ordinary skill in the art would be motivated to use a filter at the output of a phase detector to reduce voltage spikes, thereby providing the advantage of reducing transients to the motor.
- Therefore, it would be obvious to one having ordinary skill in the art at the time of the invention to modify the device of Miller so the phase detector follows a describing function, thereby providing the advantage of improving synchronous operation of the motor, as taught by Seto. Additionally, it would be obvious to one having ordinary skill in the art at the time of the invention to filter the output of the phase detector, thereby providing the advantage of reducing transients, as taught by Carobolante.
- With respect to claim 19, a person with ordinary skill in the art would know a digital phase detector and a digital loop filter could be implemented in an application specific integrated circuit (ASIC).

7. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller, Seto, and Carobolante as applied to claim 17 above, and further in view of Rhee et al (6,147,561).

   - Miller, Seto, and Carobolante do not disclose the phase frequency detector outputting positive, negative, and no current signals in response to the reference and feedback signals (claim 20), and the phase frequency detector tracks a time varying reference signal and selects the comparison signal in response to said reference signal (claim 21).
   - Rhee et al disclose the phase frequency detector outputs positive, negative, and no current (when gates #500 in fig. 5 are off) based on the reference and feedback signals (col. 6, lines 16-26); and the phase frequency detector tracks the f_{ref} value, which varies in time, to output the comparison signal (fig. 2, f_{ref} used by #14 to output #17). The motivation for a circuit as described above is to provide the advantage of enhancing the phase locked loop gain (col. 4, lines 46-57).
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the invention of Miller, Seto, and Carobolante with an integrated circuit that incorporates the components mentioned above, thereby providing the advantage of enhancing the phase locked loop gain, as taught by Rhee et al.

8. Claims 23 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami and Rhee et al as applied to claims 17 and 24 above, and further in view of Trachtenberg (6,121,747).

   - Miller, Seto, and Carobolante do not disclose the phase frequency detector having a memory.

- Trachtenberg discloses a phase frequency detector including an edge-controlled digital memory network, having a plurality of states. Further, the network makes transitions among the plurality of states responsive to the reference and feedback signals input to the comparator, and the signal generated by the comparator is dependent on the state of the network, and the automatic phasing device controls the transitions among the states (col. 7, lines 6-17). This provides the advantage of driving a low-frequency pulse modulated signal that is supplied to the motor.
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the phase frequency detector of Miller, Seto, and Carobolante with memory based on the reference signal, thereby providing the advantage of outputting a low-frequency signal to drive the motor, as taught by Trachtenberg.

Allowable Subject Matter

9. Claims 2, 5-7, 9, 22, 27, and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
   - With respect to claim 2, the Prior Art discloses feedback signals from a motor that are sent to a phase detector, and linear encoders as a movement detector that sends feedback signals. However, the primary reason for allowance is because the Prior Art does not disclose a linear optical encoder that outputs feedback signals to a digital phase detector.
   - With respect to claim 5, the Prior Art discloses state machines that receive feedback and reference signals, selectively output UP, DOWN, and no signal, output a positive current for the UP signal, output a negative current for the DOWN signal, and a high impedance

state for no signal; however, the Prior Art does not disclose a different current source for the positive and negative currents.

- With respect to claim 9, the Prior Art discloses phase frequency detectors with memory, but not with memory having weighted states.
- With respect to claims 22, 27, and 28, the Prior Art does not disclose combining into the system of Miller, Seto, and Carobolante or any other combination of references, a damping system that anticipates the motor step response to minimize the loop filter changing time.

10. Claims 11-16 and 29-31 would be allowable once the minor informalities are corrected.

- With respect to claim 11, the Prior Art discloses movement detectors/encoders that send a feedback signals to a phase detector and encoders that are attached to a carriage. However, the primary reason for allowance is because the Prior Art does not disclose an encoder attached to a carriage that sends a feedback signal to a phase detector.
- With respect to claims 29, 30, and 31, the Prior Art does not disclose combining into the system of Miller, Seto, and Carobolante or any other combination of references, a damping system that anticipates the motor step response to minimize the loop filter changing time.

KIMBERLY LOCKETT
PRIMARY EXAMINER

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Miller whose telephone number is 571-272-2070. The examiner can normally be reached on M-F, 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Nappi can be reached on 571-272-2800 ext 37. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patrick Miller
Examiner
Art Unit 2837

pm
February 16, 2004

KIMBERLY LOCKETT
PRIMARY EXAMINER

OLO

Office Action Summary	Application No. 09/440,795	Applicant(s) ADKINS ET AL.	
	Examiner Patrick Miller	Art Unit 2837	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8,10-21,23-26 and 28* is/are rejected.

7)☒ Claim(s) *5-7,9,22 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 9 and 26 are objected to because of the following informalities: See bullets below. Appropriate correction is required.

   - Claim 9 cites, "a memory." Component initially cited in claim 8. Change "a" to "the."
   - Claim 26 cites, "a corresponding comparison signal." Signal initially cited in claim 24. Change "a" to "the."

Claim Rejections - 35 USC § 103

2. Claims 1-4, 11-14, 17-21, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami (6,181,098) in view of Rhee et al (6,147,561).

   - Murakami discloses a control system and method for controlling movement of a DC motor, comprising: a movement detector to detect movement of a DC motor in an inkjet print head, including a carriage (fig. 3B, #6) attached to the motor with a belt drive (fig. 3B, #60), the motor moves the carriage (fig. 3B, #8 moves #6), and an encoder (encoder determines velocity: col. 1, lines 20-45) attached to the carriage (fig. 3B, #68), wherein the encoder outputs a feedback signal in response to the movement (and velocity) of the motor (fig. 5, output of #90).
   - Murakami does not disclose an application specific integrated circuit (ASIC) including: a digital phase detector that compares the phase of the feedback signal with a reference signal, the phase detector outputs a comparison signal based on non-linear components of the reference signal (claims 11, 18, 25), a digital loop filter, the digital phase detector is a phase frequency detector (claims 4, 12, 17,

and 24), the phase frequency detector outputting positive, negative, and no current signals in response to the reference and feedback signals (claim 13), and the phase frequency detector tracks a time varying reference signal and selects the comparison signal in response to said reference signal (claims 14 and 21).

- Rhea et al disclose an integrated circuit that performs a specific application (analogous to ASIC), wherein the application is a digital phase locked loop circuit (col. 1, lines 20-22). The circuit is comprised of a digital phase detector (phase frequency detector) (col. 4, line 50) that compares feedback with a reference signal (fig. 2, #14' compares #206 with #208), outputs a comparison signal (fig. 2, #17), the output of the phase detector follows a non-linear function (fig. 2, based on time delay elements #'s 200), and a digital loop filter (fig. 2, #20). Further, the phase frequency detector outputs positive, negative, and no current (when gates #500 in fig. 5 are off) based on the reference and feedback signals (col. 6, lines 16-26); and the phase frequency detector tracks the f_{ref} value, which varies in time, to output the comparison signal (fig. 2, f_{ref} used by #14 to output #17). The motivation for a circuit as described above is to provide the advantage of enhancing the phase locked loop gain (col. 4, lines 46-57).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the invention of Murakami with an integrated circuit that incorporates the components mentioned above, thereby providing the advantage of enhancing the phase locked loop gain, as taught by Rhee et al.

3. Claims 8, 16, 23, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami and Rhee et al as applied to claims 1, 4, 11, 12, 17, and 24 above, and further in view of Trachtenberg (6,121,747).

   - Murakami and Rhee et al do not disclose the phase frequency detector having a memory.
   - Trachtenberg discloses a phase frequency detector including an edge-controlled digital memory network, having a plurality of states. Further, the network makes transitions among the plurality of states responsive to the reference and feedback signals input to the comparator, and the signal generated by the comparator is dependent on the state of the network, and the automatic phasing device controls the transitions among the states (col. 7, lines 6-17). This provides the advantage of driving a low-frequency pulse modulated signal that is supplied to the motor.
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the phase frequency detector of Murakami and Rhee et al with memory based on the reference signal, thereby providing the advantage of outputting a low-frequency signal to drive the motor, as taught by Trachtenberg.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami and Rhee et al as applied to claim 1 above, and further in view of Lundberg et al (5,811,998).

   - Rhee et al disclose the digital phase detector being a phase frequency detector; however, Murakami and Rhee et al do not disclose the digital filter being a compensator that is set by a digital clock.

- Lundberg et al disclose a digital filter that is an up/down counter configured to function as a digital integrator (digital compensator) (fig. 6, #138 including #140), whereby the digital integrator is controlled by a clock (fig. 6, #139). The motivation to provide a digital integrator as described is to integrate the occurrences of the phase condition. This provides the advantage of enabling phase expansion (col. 7, lines 14-25).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention that the digital filter of Murakami and Rhee et al could be a digital integrator (compensator), thereby providing the advantage of enabling phase expansion, as taught by Lundberg et al.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami and Rhee et al as applied to claims 11 and 12 above, and further in view of Rogers (5,371,425).
   - Murakami and Rhee et al do not disclose the phase frequency detector providing for system damping.
   - Rogers discloses a circuit where the phase frequency detector is included in a digital damping circuit. The motivation to provide a circuit as disclosed by Roger is to have a digital damping circuit, which generates adequate phase and frequency damping without a damping resistor. This provides the advantage of achieving damping effects, which are unaffected by process parameters and operating and ambient parameters (abstract).
   - Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to make the phase frequency detector of Murakami and

Rhee et al for system damping, thereby providing the advantage of achieving damping effects that are unaffected by process parameters and operating ambient parameters, as taught by Rogers.

6. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murakami (6,181,098) in view of Tanaka (5,452,326).

- Murakami discloses a control system and method for controlling movement of a DC motor, comprising: a movement detector to detect movement of a DC motor in an inkjet print head, including a carriage (fig. 3B, #6) attached to the motor with a belt drive (fig. 3B, #60), the motor moves the carriage (fig. 3B, #8 moves #6), and an encoder (encoder determines velocity: col. 1, lines 20-45) attached to the carriage (fig. 3B, #68), wherein the encoder outputs a feedback signal in response to the movement (and velocity) of the motor (fig. 5, output of #90).
- Murakami does not disclose modeling the phase detector in a closed loop, phase locked loop configuration with a describing function; and dampening the frequency response of the describing function by anticipating a step response of the motor during initial movement.
- Tanaka discloses a digital phase locked loop circuit that provides damping features as cited above. The motivation to provide a circuit as cited is to provide the advantage of improving excess response to a step response (col. 6, lines 47-68).
- Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify the system of Murakami so the circuit is configured to carry out phase locked loop operations and dampen the frequency

response as cited above, thereby providing the advantage of improving system excess response, as taught by Tanaka.

Allowable Subject Matter

7. Claims 5-7, 9,

8. 22, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

- With respect to claim 5, the Prior Art discloses state machines that receive feedback and reference signals, selectively output UP, DOWN, and no signal, output a positive current for the UP signal, output a negative current for the DOWN signal, and a high impedance state for no signal; however, the Prior Art does not disclose a different current source for the positive and negative currents.
- With respect to claim 9, the Prior Art discloses phase frequency detectors with memory, but not with memory having weighted states.
- With respect to claims 22 and 27, the Prior Art does not disclose combining into the system of Murakami and Rhee et al, nor any other combination of references, a damping system that anticipates the motor step response to minimize the loop filter changing time.

Prior Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Williams (5,818,272) discloses a non-linear phase locked loop circuit with a phase detector and a pulse filter (integrator).

- Powell (5,790,614) discloses a digital system with a phase detector and a loop filter.
- Yokoi et al (5,873,663) disclose a printing apparatus that has a detector for measuring the carriage moving speed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick Miller whose telephone number is 703-308-4931. The examiner can normally be reached on M-F, 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Nappi can be reached on 703-308-3370. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Patrick Miller
Examiner
Art Unit 2837

pm
August 7, 2003

ROBERT E. NAPPI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800